**Course Outline: EE1005 Digital Logic Design**

**Program:** BS Computer Science

**Semester:** Spring 2023

**Credit Hours: 3**

**Pre-requisite(s): None**

**Instructor:** Dr. Suleman Mir

**Course Description:**

This course has been designed to understand the fundamental concepts in classical digital design and to demonstrate how digital circuits are designed and analyzed today. This course helps in developing the ability to design both combinational and sequential digital logic circuits. It familiarizes with the modern hierarchy of digital hardware and enlightens the state-of-the-art computer hardware design methodologies.

**Text & Reference Book(s):**

**Text:** Digital Fundamentals by Thomas L. Floyd, Latest Edition, Pearson.

**Reference:** Logic & Computer Design Fundamentals by M. Morris Mano & Charles R. Kime, Latest Edition, Pearson

**Assessment Plan:**

|  |  |
| --- | --- |
| Quizzes (3) 6 % |  |
| Assignments (3) 6 % |  |
| Project 8 % |  |
| Sessional I 15 % Sessional II 15 % |  |
| Final exam 50%  Total 100% |  |
|  |  |
|  |  |

**Program Learning Outcomes:**

Students are expected to achieve the following PLOs in this course.

**PLO-1:** **Engineering Knowledge:** An ability to apply knowledge of mathematics, science and engineering to the solution of complex engineering problems. (**WK1 to WK4**)

**PLO-3:** **Design/Development of Solutions:** An ability to design solutions for complex engineering problems and design systems, components or processes that meet specified needs with appropriate consideration for public health and safety, cultural, societal, and environmental considerations. (**WK5**)

**Course Learning Outcomes:**

Upon successful completion of this course, students will be able to:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S.No** | **CLO** | **Domain** | **Taxonomy level** | **PLO** | **Assessment Tool** |
| 1. | **Solve** different number systems and **Examine** basic logic gates & **Solve** simple logics using Boolean algebra and Karnaugh Maps. | Cognitive | 3 | 1 | A1, Q1, S1, F1 |
| 2. | **Design** combinational circuits using Encoders, Decoders, Multiplexers, Demultiplexers, Adders and Multipliers. | Cognitive | 5 | 3 | A2, Q2, S2, ,P1,F2 |
| 3. | **Develop** Sequential Logic Circuits (SLC’s) using different types of flip-flops and **Design** SLC’s used in typical digital systems. | Cognitive | 5 | 3 | A3, Q3,P2, F3 |

*A = Assignment, Q = Quiz, S= Sessional, F = Final, P = Project, W = Written Report*

**Course Contents:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Week** | **Topics to be Covered** | **Chapter** | **CLO** |
| 1 | * Digital vs. Analog * Binary digits, Logic Levels and Digital Waveforms * Introduction to Basic Logic operations * Overview of Logic functions * Integrated circuit Technologies | 1 | 1 |
| 2-3 | * Number Systems (2,8,10,16) and base conversions * Binary Arithmetic * I’s and 2’s complements * Signed numbers * Floating point numbers * BCD, ASCII, Gray codes, parity * Logic gates | 2  3 | 1 |
| 4-5 | * Boolean Operations and Expressions, theorems of Boolean Algebra, De-Morgan’s Theorems, Boolean Analysis of Logic Circuits * Simplification using Boolean Algebra * Standard forms of Boolean Expressions * Boolean Expressions and Truth Tables * The KARNAUGH MAP * KARNAUGH MAP SOP Minimization   KARNAUGH MAP POS Minimization | 4  4 | 1 |
| 6-8 | * Basic combinational Logic Circuits and Implementation * Universal properties and combinational logic of NAND and NOR gates * Adders * Comparators * Decoders * Encoders * Code Converters * Multiplexers and Demultiplexers * Parity generators/checkers * Latch | 5  6  7 | 2 |
| 9-10 | * Sequential Circuits * Basic Memory Elements * SR Latch Using NOR, SR Latch Using NAND * Difference between Latch and Flip Flop, Basic SR Flip Flop * D Flip Flop * JK Flip Flop * Edge Triggered Flip Flops * Flip Flops and Timing Diagrams, Using Flip Flops as Frequency Divider Circuit | 7  7 | 2,3 |
| 11-16 | * Shift Registers * Counters | 8  9 | 3 |